APPLICATION OF SOFT COMPUTING TOOLS FOR BETTER NANODEVICE MODELING AND THEIR APPLICATIONS IN DIGITAL CIRCUITS

THESIS

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Synopsis

Continued device performance improvement is possible only through a combination of device scaling with new device structure and or new material to its fundamental limits, determined by manufacturing physics and cost using new materials and non classic structures. To extract the best performance from a device it is very essential to choose the parameters intelligently as the performance is controlled by them. Hence to predict the best parameters at a time it is better to think over some special computational methods. As an attempt towards such computing, adaptive intelligent controls, by neural networks are deployed here, in the chapter 2, to predict the device parameters so as to get the best performance from the device. A soft computing tool, Artificial Neural Network (ANN), is used in the present work to get optimized system parameters of GaAs quantum wells for desired device characteristics.

Low dimensional structures, also called nanostructures, provide opportunities to realize high speed, low power consuming devices. The quantization of electron motion in systems of reduced dimensionality brings about different features in the electron kinetics compared with those available in the bulk devices. The biasing field, lattice temperature and system parameters play a crucial role in predicting the device

performance. The values of the system parameters, biasing field and lattice temperature can be optimized to get the desired response from a device.

The aim of the chapter 3 is to predict the optimum values of the system parameters of the GaAs and $In_{0.53}Ga_{0.47}As$ quantum walls (QWs), called, nanostructures incorporating the relevant scattering mechanisms and the effect of the longitudinal optic phonons using heated drifted Fermi-Dirac distribution function. A soft computing tool Genetic Algorithm has been deployed here for this purpose.

In this work a neural network is employed to optimize and predict various system parameters, dc biasing field, frequency at which the quantum structure will provide better performance. GaAs quantum well structures have been deployed for such prediction. The present model depicts the error in prediction to provide certain flexibility in the system parameters with no significant deviation from the desired characteristics of the proposed device. The prevailing connectionist approach today is originally known as Parallel Distributed Processing (PDP). PDP is a neural network approach that stresses the parallel nature of neural processing, and the distributed nature of neural representations. PDP provides a general mathematical framework for researchers to operate in. With the use of parallel network architecture the training time is much reduced. In parallel neural network architecture the training data set is divided into equal number of blocks each of which is fed to each network in the parallel

architecture. This simultaneously trains all the networks in the architecture thus lowering down the training time of the architecture. Chapter 4 deals with all those mentioned above for (In,Ga)As quantum nanostructure.

Conventional, silicon-based electronics is seriously challenged by modern computers for forcing researchers to explore unfamiliar territory in the quest for increased performance in the line of processor speed, memory storage capacity and power consumption. In recent years, there has been a considerable interest among the researchers for correlated single-electron tunneling based on coulomb blockade effect in ultra small structures, called nanostructures. In the chapter 5 a single electron threshold logic based automatic Drinking Water Machine has been designed and its performance on a computer based model is studied with satisfactory response thereby establishing the feasibility of much faster VLSI circuits. We can apply soft computing tool to reduce the components needed to realize the circuit. The soft computing can also be used to optimize the wire length to reduce the chip area. This part of the work is not completed. The candidate has summed up, in chapter 6, the outcome and the conclusions of the present study.